

Features:

- n Isolated mounting base 3000V~
- n Solder joint technology with increased power cycling capability
- n Space and weight saving

Typical Applications

- n AC/DC Motor drives
- n Various rectifiers
- n DC supply for PWM inverter

V_{DSM}, V_{RSM}	V_{DRM}, V_{RRM}	Type & Outline
900V	800V	MFC90-08-224H3
1100V	1000V	MFC90-10-224H3
1300V	1200V	MFC90-12-224H3
1500V	1400V	MFC90-14-224H3
1700V	1600V	MFC90-16-224H3
1900V	1800V	MFC90-18-224H3

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	$T_j(^{\circ}C)$	VALUE			UNIT
				Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Single side cooled, $T_c = 85^{\circ}C$	125			90	A
$I_{T(RMS)}$	RMS on-state current		125			141	A
I_{DRM} I_{RRM}	Repetitive peak current	at V_{DRM} at V_{RRM}	125			20	mA
I_{TSM}	Surge on-state current	10ms half sine wave	125			1.9	kA
I^2t	I^2t for fusing coordination	$V_R = 60\% V_{RRM}$				18.1	$A^2s \cdot 10^3$
V_{TO}	Threshold voltage		125			0.70	V
r_T	On-state slope resistance					3.01	mΩ
V_{TM}	Peak on-state voltage	$I_{TM} = 270A$	25			1.80	V
dv/dt	Critical rate of rise of off-state voltage	$V_{DM} = 67\% V_{DRM}$	125			1000	V/μs
di/dt	Critical rate of rise of on-state current	Gate source 1.5A $t_r \leq 0.5\mu s$ Repetitive	125			200	A/μs
I_{GT}	Gate trigger current	$V_A = 12V, I_A = 1A$	25	30		200	mA
V_{GT}	Gate trigger voltage			0.6		2.5	V
I_H	Holding current			10		250	mA
V_{GD}	Non-trigger gate voltage	$V_{DM} = 67\% V_{DRM}$	125			0.2	V
$R_{th(j-c)}$	Thermal resistance Junction to case	Single side cooled per chip				0.28	$^{\circ}C/W$
$R_{th(c-h)}$	Thermal resistance case to heatsink	Single side cooled per chip				0.15	$^{\circ}C/W$
V_{iso}	Isolation voltage	50Hz, R.M.S, $t = 1min, I_{iso} : 1mA(MAX)$		3000			V
F_m	Thermal connection torque(M5)			2.5		4.0	N-m
	Mounting torque(M6)			4.5		6.0	N-m
T_{vj}	Junction temperature			-40		125	$^{\circ}C$
T_{stg}	Stored temperature			-40		125	$^{\circ}C$
W_t	Weight				100		g
Outline	224H3						

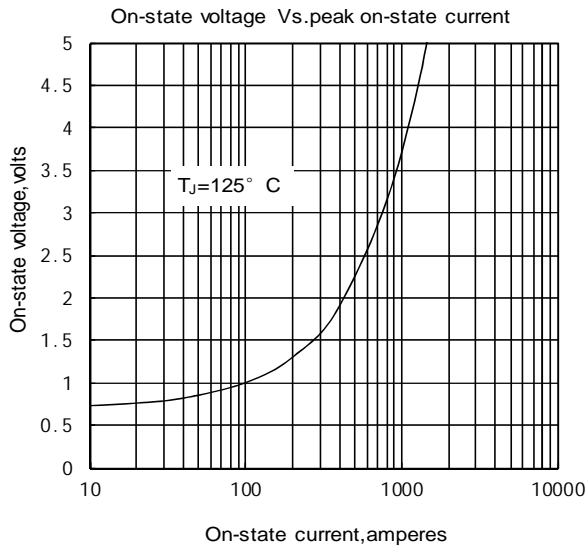


Fig1

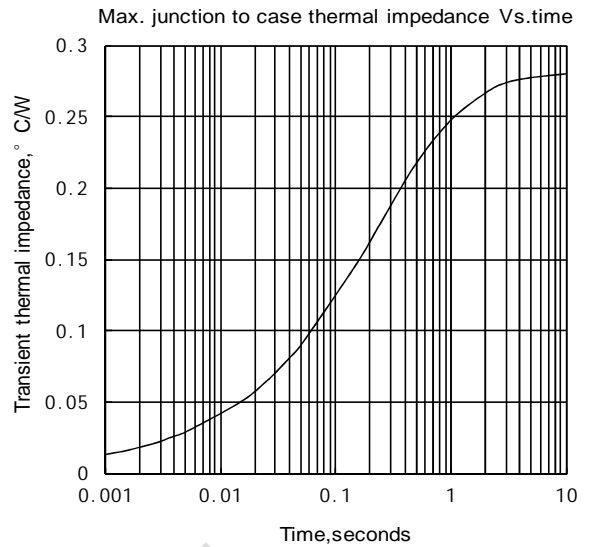


Fig2

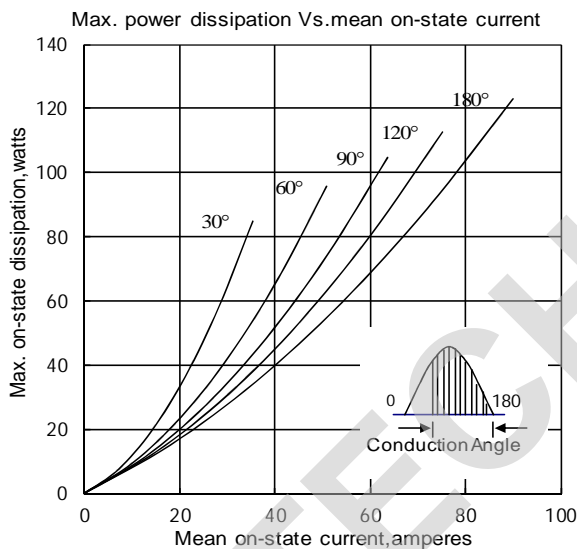


Fig3

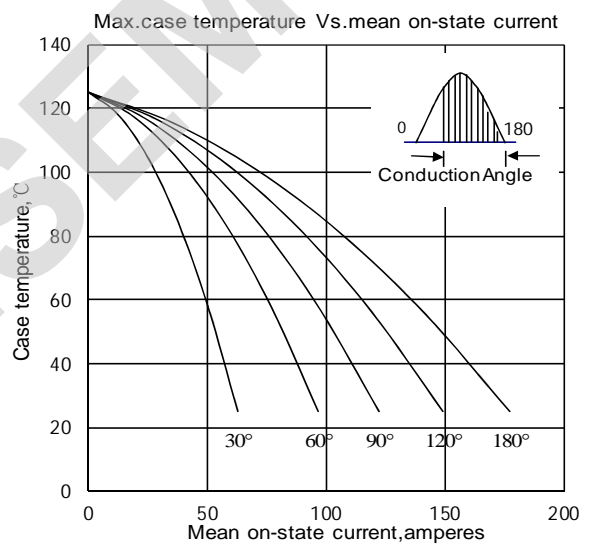


Fig4

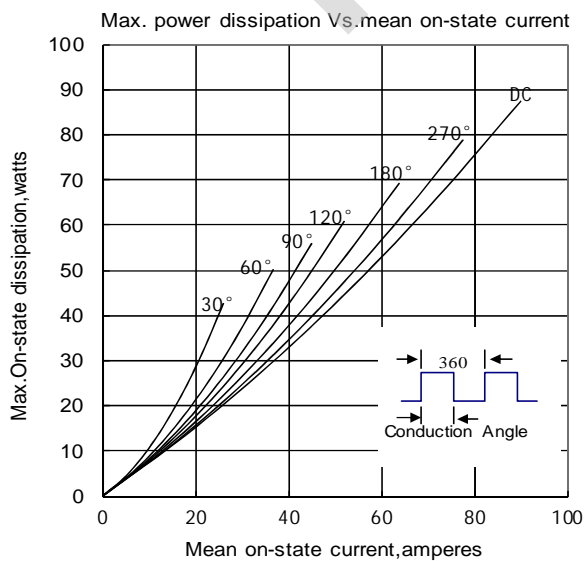


Fig5

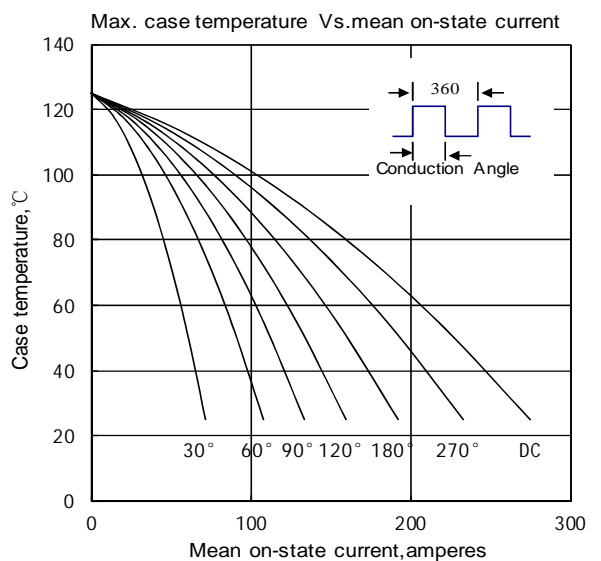


Fig6

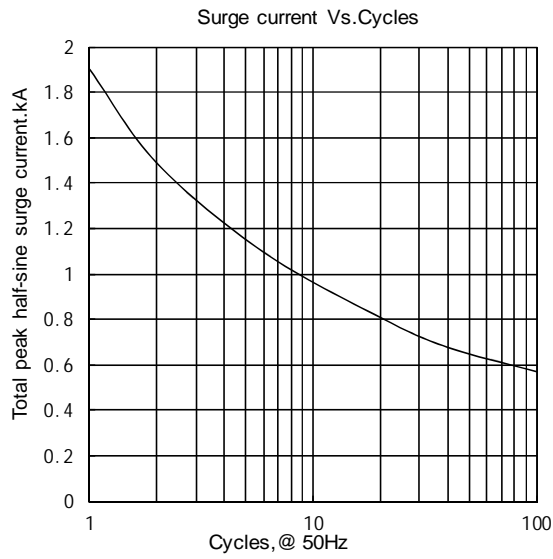


Fig7

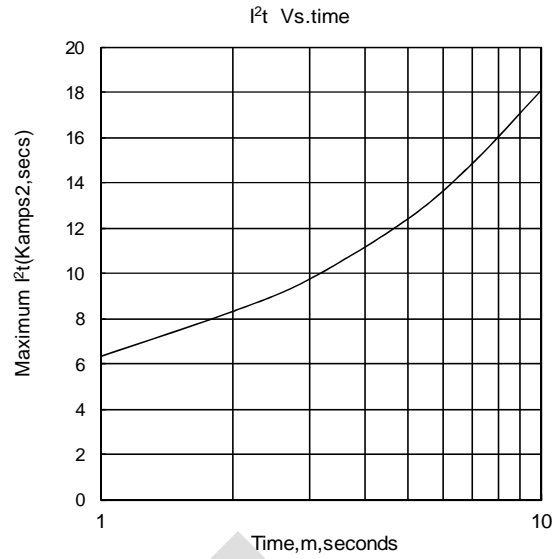
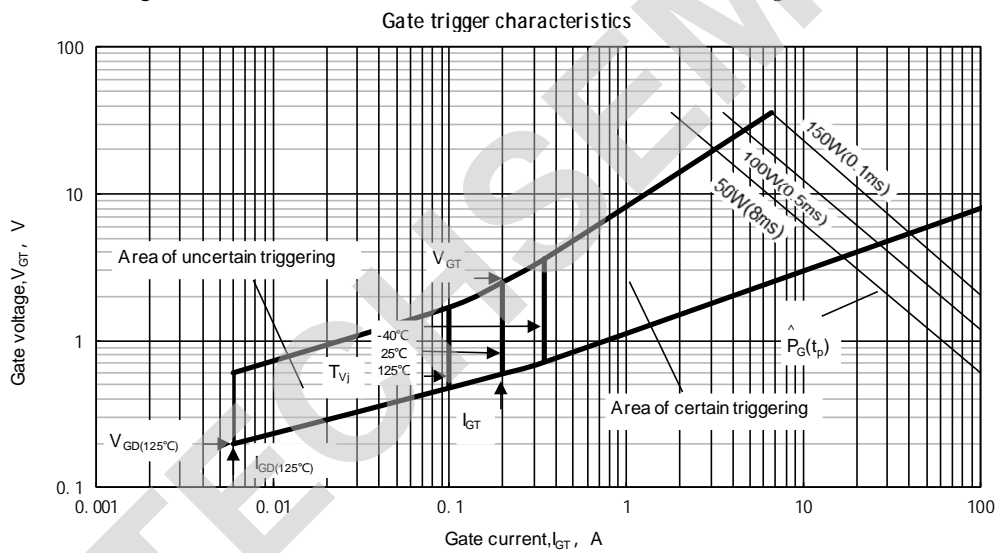


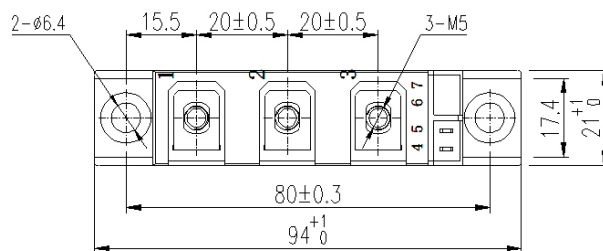
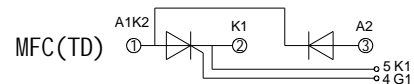
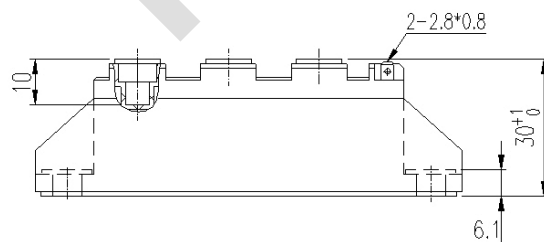
Fig8



Gate trigger characteristics

Fig.9

Outline:



Unmarked dimensional tolerance: $\pm 0.5\text{mm}$

TECHSEM reserves the right to change specifications without notice.