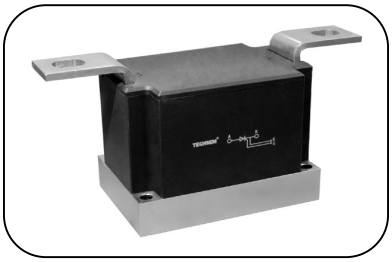


Features：

- **n** Isolated mounting base 4000V~
- **n** Pressure contact technology with Increased power cycling capability
- **n** Space and weight saving

Typical Applications

- **n** AC/DC Motor drives
- **n** Various rectifiers
- **n** DC supply for PWM inverter

V_{DSM},V_{RSM}	V_{DRM},V_{RRM}	Type & Outline
2700V	2600V	MT600-26-432F2
2900V	2800V	MT600-28-432F2
3100V	3000V	MT600-30-432F2
3300V	3200V	MT600-32-432F2
3500V	3400V	MT600-34-432F2
3700V	3600V	MT600-36-432F2

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T_j(°C)	VALUE			UNIT
				Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Single side cooled, T_c=85°C	125			600	A
$I_{T(RMS)}$	RMS on-state current					942	A
I_{DRM} I_{RRM}	Repetitive peak current	at V_{DRM} at V_{RRM}	125			80	mA
I_{TSM}	Surge on-state current	10ms half sine wave V_R=60%V_{RRM}	125			16	kA
I^2t	I^2t for fusing coordination					1280	10^3A^2s
V_{TO}	Threshold voltage		125			0.92	V
r_T	On-state slope resistance					0.45	mΩ
V_{TM}	Peak on-state voltage	I_{TM}=1800A	25			2.24	V
dv/dt	Critical rate of rise of off-state voltage	V_{DM}=67%V_{DRM}	125			1000	V/μs
di/dt	Critical rate of rise of on-state current	Gate source 1.5A t_r≤0.5μs Repetitive	125			200	A/μs
I_{GT}	Gate trigger current	V_A=12V, I_A=1A	25	30		200	mA
V_{GT}	Gate trigger voltage			0.8		3.0	V
I_H	Holding current			10		200	mA
V_{GD}	Non-trigger gate voltage	V_{DM}=67%V_{DRM}	125			0.2	V
$R_{th(j-c)}$	Thermal resistance Junction to case	Single side cooled per chip				0.042	°C /W
$R_{th(c-h)}$	Thermal resistance case to heatsink	Single side cooled per chip				0.015	°C /W
V_{iso}	Isolation voltage	50Hz,R.M.S,t=1min,I_{iso}:1mA(MAX)		4000			V
F_m	Terminal connection torque(M12)			12.0		14.0	N·m
	Mounting torque(M6)			4.5		6.0	N·m
T_{vj}	Junction temperature			-40		125	°C
T_{stg}	Stored temperature			-40		125	°C
W_t	Weight				2700		g
Outline	432F2						

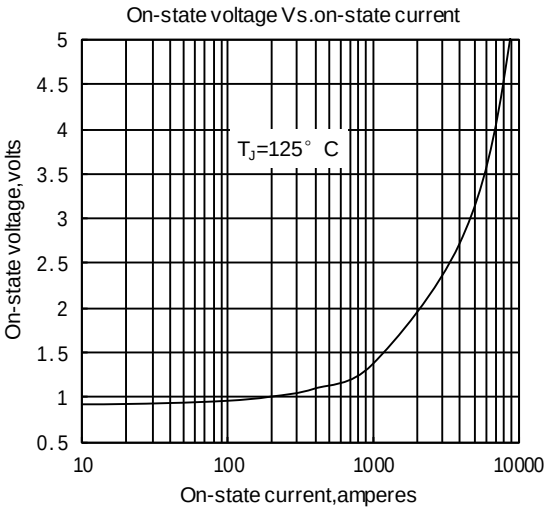


Fig.1

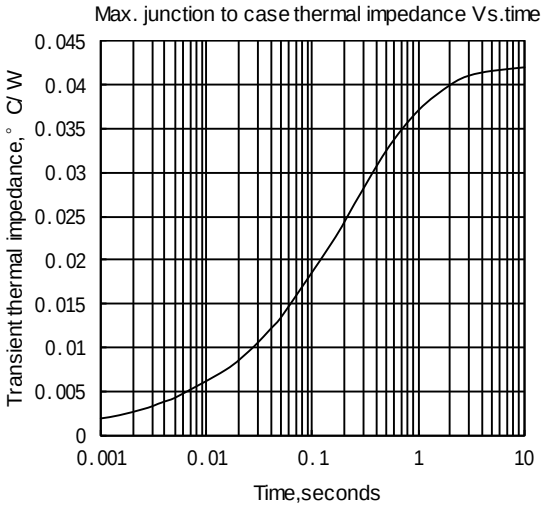


Fig.2

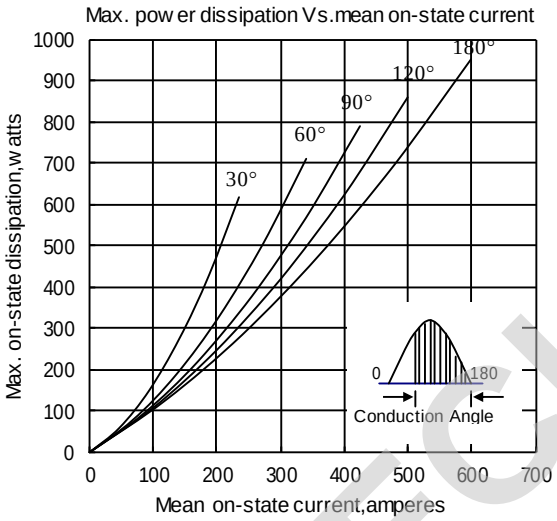


Fig.3

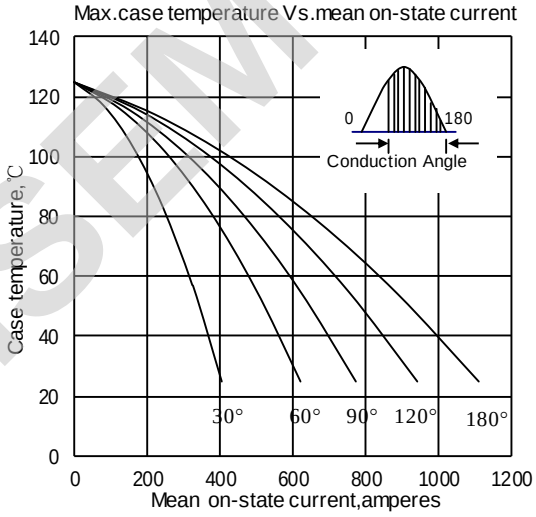


Fig.4

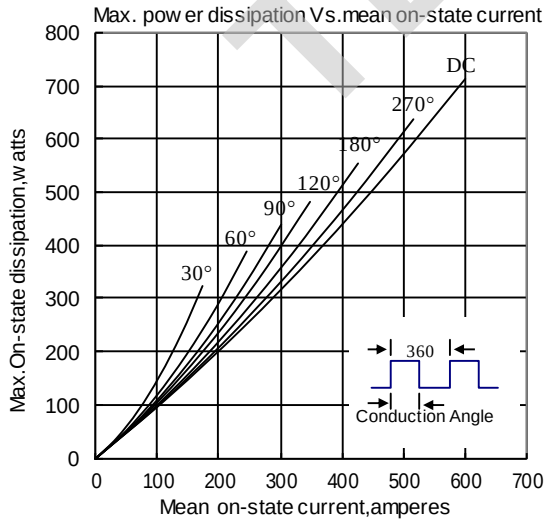


Fig.5

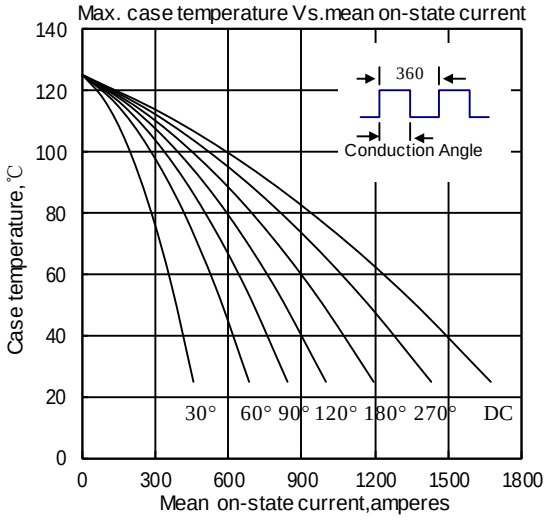


Fig.6

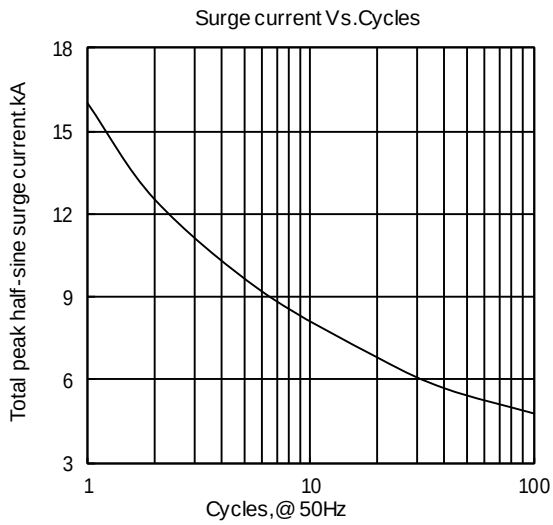


Fig.7

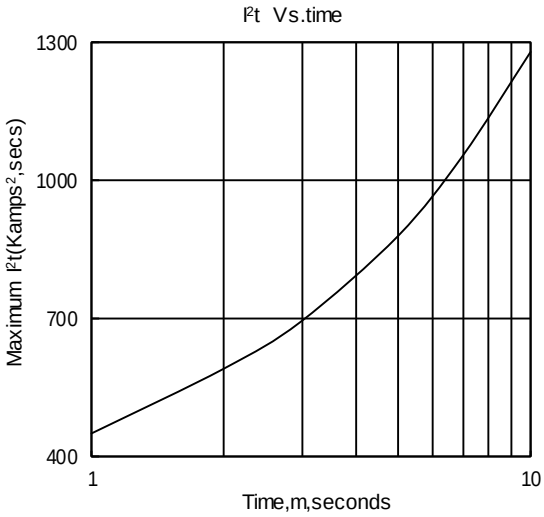


Fig.8

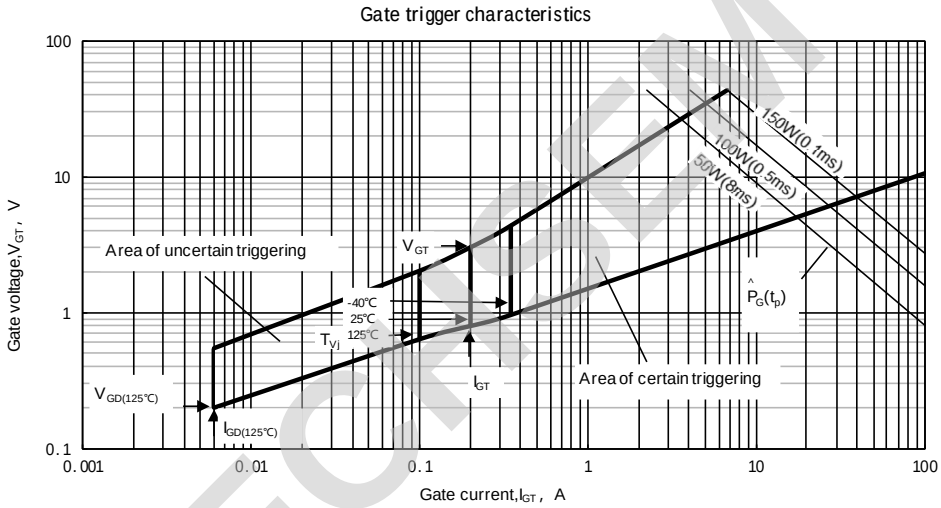
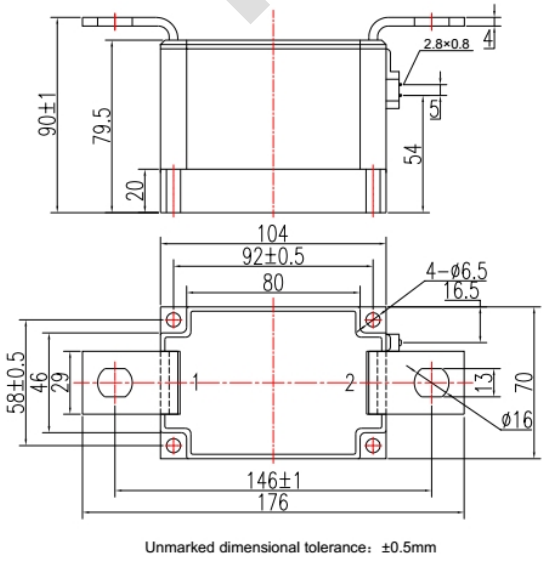


Fig.9

Outline:



Unmarked dimensional tolerance：±0.5mm